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NUMERICAL STUDY ON SOME IMPROVEMENTS IN THE PASSIVE COOLING SYSTEM OF A RADIO BASE STATION

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Passive cooling schemes, such as natural convection, are the most safe heat dissipation mode of electronic equipment. Some times the highest temperature of the PCB, rather than the highest of chips, is very much a concern due to technological reasons. In order to reduce the maximum PCB temperature, this article discusses various improvement methods via numerical simulation. These include optimization of fin number of heat sink, structure improvement of sun shield, and creation of insulation cavity in the base plate of heat sink. Taking the PCB of an RBS as an example, numerical simulation results show that by integrating these methods the maximum PCB temperature can be appreciably reduced. This article provides an example that by using a careful numerical thermal design, a passive cooling mode can sometimes meet the cooling requirement of a PCB with high power input in some extent.

1. INTRODUCTION

With performance improvement and size reduction of electronic devices, their power dissipation level and power density significantly increase, which leads to a more deteriorated temperature environment affecting their performance. More effective heat dissipation techniques are required, and thermal management has already become one of the key aspects for ensuring the performance and reliability of high power components. This article mainly focuses on the passive cooling performance of a printed circuit board (PCB) of a radio base station (RBS).

Passive cooling schemes, such as natural convection, are the most general heat dissipation modes of electronic equipment. Compared with active heat dissipation, such as forced air convection, thermoelectric cooler and water cooling, it has a simpler structure and does not depend on external action, such as power, water, or others to maintain a cooling function. Therefore a passive cooling mode always

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NOMENCLATURE

a	space between top of RBS and bottom of sun shield top board, m	T	temperature, °C
b	thickness of RBS, m	u, v, w	velocity components in x, y, z directions, m/s
H'	critical elevation angle, rad	U	velocity vector (u, v, w), m/s
g	acceleration of gravity, m/s^2	x, y, z	Cartesian coordinates
Gr^*	modified Grashof number, $Gr^* = g\beta QL^4/(\lambda\nu^2)$	β	thermal expansion coefficient, K^{-1}
		ε_ϕ	specified small value for determining convergence
I	length of RBS, m		
L	characteristic length, m	λ	fluid thermal conductivity, $W/(m \cdot K)$
m	length of jalousie of the grill sun shield, m	v	fluid kinematic viscosity, m^2/s
n	space between jalousies of the grill sun shield, m	ρ	density, kg/m^3
		Γ_ϕ	generalized diffusion coefficient
p	space between jalousies and RBS, m	ϕ	general variable
P	fluid pressure, Pa	**Subscripts**	
q	jalousie plate thickness, m	∞	external condition
Q	heat flux, W/m^2	max	maximum value
S	number of jalousie(s) of the grille sun shield	mean	average value
		min	minimum value
S	generalized source term	ϕ	general variable

has better reliability and longer service life. It is very suitable for electronic devices, such as RBS and LED (light emitting diode) lamp, which requires a long lifetime and serves for long-term unattended duty. Alternatively, passive cooling is usually characterized by low heat flux. Thus, it is especially necessary and important to explore the potential of passive cooling to meet the need of dissipating required power and heat flux.

Publications in passive thermal management are quite limited in the open literature. Recently three related articles have been published and are briefly introduced as follows. Chiriac and Lee [1] investigated several system level variables in a general packet radio service (GPRS) mobile telephone, including the PCB thermal-via distribution, power management package designs, and enclosure convection and thermal interaction among packages. Osone [2] investigated the thermal performance of a power semiconductor module used in mobile communication systems, and found that the thickness of the semiconductor substrate, the thickness of the multi-layer PCB, the thermal conductivity of the bonding material under the semiconductor substrate, and misalignment of thermal vias between each layer of PCB were the most important factors affecting the thermal resistance of the module. Recently, Moon et al. [3] discussed various passive thermal management schemes for a high power component in a handheld electronic device, and evaluated the effects of passive thermal solution options via conduction and natural convection enhancements, by utilizing the validated system mock-up model and the system level test unit with a ball grid array (BGA) type of three-die stacked chip-scale package (SCSP).

The abovementioned research all focused on low power electronic equipment (mobile phone), whose power is lower than 10 W.

In this study, the system thermal design of a kind of outdoor radio base station (RBS) with a total power input of 132.5 W is investigated, and its significant

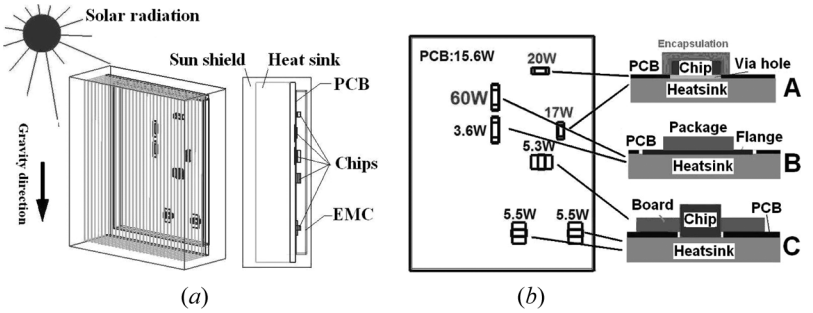


Figure 1. Schematic diagram of the RBS. (*a*) Configuration and working state of the RBS; and (*b*) heat dissipation on the PCB.

parameters are optimized by means of the commercial software ICEPACK. Various passive thermal management schemes by enhancing conduction, radiation, and natural convection are implemented and discussed. The major purpose for the thermal design is to limit the maximum temperature of PCB equal or less than 85°C, which is required from some technological point of view described later.

2. PROBLEM DESCRIPTION

A schematic diagram of the configuration and working environment of the RBS are shown in Figure 1*a*. The RBS works outdoors. As shown, the PCB of the RBS is attached to a heat sink, all chips are located on the other side of the PCB, and an electromagnetic cover (EMC) is used to cover the PCB and chips. A sun shield is installed outside of heat sink for obstructing solar radiation.

The designed ambient temperature is +55°C, which is the most critical ambient temperature. The highest temperature of any spot in the PCB should be less than +85°C, except the heat source chips, and as low as possible. This is because the solder joint on the PCB may fail by thermal stress when the operating temperature is higher than +85°C, while the operating temperature of a chip may be relatively higher. For instance, the maximum operating junction temperature of a radio frequency (RF) power field effect transistor is allowed to be as high as +200°C. The hot spot on the PCB should be reduced at passive cooling condition. For the present study, the size of the heat sink width and length should be less than 275 and 340 mm, respectively. The weight of the heat sink and the cost of manufacturing should be as low as possible. It is worth mentioning that the model and all the above conditions are extracted from a real RBS, which has been practically used.

3. PHYSICAL MODEL AND MATHEMATICAL FORMULATION

3.1. Physical Model

The details of the heat sources studied are first described as follows, which are copied from the practical RBS in usage. The total power generation of the RBS is 132.5 W, and heat sources of the RBS are the PCB and the chips on it. The positions

Table 1. External dimensions and thermophysical properties of chips

Component type		Dimension (mm)	Thermal conductivity (W/(m · K))
PCB		$245 \times 311 \times 1.2$	Tangential of board: 20 Normal of board: 1
A-type chips	Encapsulation	$23 \times 9 \times 2.5$	0.2
	Chip	$17 \times 7 \times 1.8$	205
	Via hole	$17 \times 7 \times 1.2$	Tangential of board: 1 Normal of board: 12
B-type chips	Package	$9 \times 20 \times 2$	200
	Flange	$9 \times 33 \times 1.2$	205
C-type chips	Chip	$9 \times 18 \times 7.2$	2.5
	Board	$28 \times 18 \times 3$	1

and power generation of the heating chips can be seen in Figure 1*b*. It should be noted that the PCB power of 15.6 W is from other distributed heat sources set up on the entire PCB and is assumed uniformly distributed over PCB for the convenience of simulation. The main power elements have three kinds of packaging A-type, B-type, and C-type, as shown in the figure. The A-type package includes the encapsulations of a 20 W chip and 17 W chip, which are a kind of small outline package (SOP). They are assembled on the PCB by chip side feet and via holes perforated in the region of the PCB touched to the chip for enhancing heat dissipation. The chips of 60 W and 3.6 W are of a B-type element structure, which are a kind of RF power field effect transistors, whose packaging and connection mode will be discussed in section 5.5. The 60 W chip is the largest power generation chip studied, and its heat flux is up to $3.33 \times 10^5\,\mathrm{W/m^2}$, which provides the biggest challenge in the passive thermal management of this study. The 5.3 W chip and two 5.5 W chips are connected with a heat sink through the holes of the PCB, which belong to the C-type element configuration in Figure 1*b*.

For a rapid thermal design of the RBS and minimizing the number of grids while still keeping the basic features of the RBS studied, the following assumptions were made for the physical model. (1) Apart from the three types of heat sources, the rest of the PCB is taken as a smooth plate with pre-specified thermal conductivity; (2) the basic structures of the three types of heat sources are modeled, as shown by their cross-section picture in Figure 1*b*; (3) the air flow is considered to be incompressible and turbulent; (4) the heat transfer process is in a steady state and all of the thermophysical properties are constant, except the air density in the gravitational term, which will be modeled by the Boussinesq assumption [4]. The external dimensions and thermophysical properties of the three types of chips provided by the manufacturer are listed in Table 1.

3.2. Mathematical Formulation

3.2.1. Governing equations. For the problem at hand the natural convective heat transfer, conduction in the PCB, and radiation heat transfer have to be taken into account simultaneously, making the problem a complicated conjugate one.

According to the above assumptions, the governing equations for the convective-conductive heat transfer may be expressed as follows [5].

$$\mathrm{div}(\rho U\phi) = \mathrm{div}(\Gamma_\phi \mathrm{grad}\phi) + S_\phi \tag{1}$$

where ϕ is a general variable, which can represent the following solved variables: u, v, w, and T; Γ_ϕ is the generalized diffusion coefficient; and S_ϕ is the generalized source term.

Because the radiative heat transfer plays an important role when an electric device is cooled by natural convection, the radiative heat transfer is taken into account in the numerical simulation. The air is assumed to be nonparticipating in the radiation, and all of the solid surfaces including chips, PCB, EMC cover, heat-sink, and sun-shield are assumed to be gray and diffuse. The surface-to-surface radiation model in Icepak [6] has been used here. The net radiative heat transfer rate is taken as the additional sources applied only to the cells adjacent to the interface of gas and solid. The derivation and implement process of the additional sources can be referred to in references [7–10].

3.2.2. Numerical method. The above governing equations are discretized by the finite-volume method [5, 11]. The coupling between pressure and velocity is implemented by the SIMPLE algorithm. The convection term is discretized by the second-order upwind difference scheme, and the diffusion term is discretized by the central difference scheme. Mesh generation and numerical calculation are performed by the commercial CFD software Icepack [6].

3.2.3. Boundary condition specification. Boundary conditions are an indispensable part of the mathematical solution of the governing equations. Theoretically, the computational domain for the problem at hand is an infinite space because of the natural convection. Practically, we can only simulate a finite large enough space. The outer boundary of such a space is called pseudo-outer boundary and its determination will be presented later. At the pseudo-outer boundary, the following conditions are established: $P = 101325\,\mathrm{Pa}$, $T = T\infty = 55^\circ\mathrm{C}$; $u = 0$, and $v = 0$ (at upper and lower boundaries); $v = 0$, $w = 0$ (at left and right boundaries); $u = 0$, and $w = 0$ (at front and rear boundaries). The specific power input of each chip is given to the corresponding numerical model as its source term.

According to the models described above, a coupled solution method is adopted which means that the temperature field in the solid and flow regimes is calculated simultaneously. The numerical simulation is conducted for the entire computational domain, with the solid region being treated as a special liquid. To achieve it, the harmonic mean method is used to determine the diffusion coefficient at the control volume interface. The thermal conductivity at the different material regions should adopt individual values to keep the heat flux continuum at the interface, while the heat capacity of fluid is used for all fluid and solid regions because the nominal diffusion coefficient in the energy equation is λ/c_p rather than itself λ[6, 12].

During the iterative solution process, if the relative deviation between two consecutive iterations is less than the specified small value ε_ϕ, the iteration is considered converged.

$$\max\left(|\phi^n_{i,j,k} - \phi^{n-1}_{i,j,k}| \Big/ |\phi^n_{i,j,k}|\right) < \varepsilon_\phi \tag{2}$$

where ϕ represents the variables u, v, w, and T; ε_ϕ equals 10^{-5} and 10^{-9} for flow and energy, respectively.

3.2.4. Turbulence model. In order to verify that turbulent flow assumption is reasonable, some preliminary evaluation was conducted. According to references [13, 14], the Grashof number is the criterion to judge whether a natural convection flow is turbulent or not. For electronic cooling, the thermal boundary condition of the PCB is best described by a uniformly heated surface [15], and the following modified Grashof number should be used.

$$\mathrm{Gr}^* = \frac{g\beta Q L^4}{\lambda \nu^2} \tag{3}$$

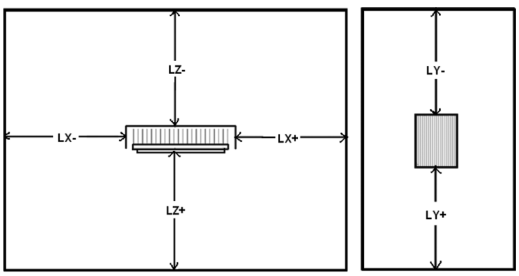
where g is the acceleration of gravity, β is thermal expansion coefficient, Q is heat flux, L is the characteristic length which takes value as heat sink length, λ is the fluid thermal conductivity, and ν is the fluid kinematic viscosity.

The modified Grashof numbers of the RBS is within the transition range of $3 \times 10^9 \leq \mathrm{Gr}^* \leq 2 \times 10^{10}$, therefore a turbulent model is best used in the governing equations. In this regard, the standard κ-ϵ turbulence mode is adopted.

4. VERIFICATION AND VALIDATION OF MODEL

4.1. Computational Domain Verification

As indicated above, the RBS works outdoors and this enables the device to have enough space for air flow and heat transfer to be developed. From the heat transfer theory, this is the natural convection in an infinite space [13, 14]. However, in the numerical simulation only a finite computational domain can be accepted. Thus, the computational domain specification is very important which should make the RBS in the study surrounded by infinite space. From a numerical simulation standpoints the appropriate computational domain should be in such a condition that the numerical results are almost independent of its size, and its further expansion leads to an ignorable effect on the numerical results. Five different computational domains are numericaly tested to study their influence on the highest



(*a*) Top View (*b*) Side View

Figure 2. Computational domain verification.

Table 2. Influence of computational domain on T_{max} of the PCB

Item	Biggest	Bigger	Adopted	Smaller	Smallest
Definition	$Lx- = Lx+ = 4L$ $Ly- = Ly+ = 6L$ $Lz- = Lz+ = 4L$	$Lx- = Lx+ = 2L$ $Ly- = Ly+ = 3L$ $Lz- = Lz+ = 2L$	$Lx- = Lx+ = L$ $Ly- = Ly+ = 2L$ $Lz- = Lz+ = L$	$Lx- = Lx+ = L/2$ $Ly- = Ly+ = L$ $Lz- = Lz+ = L/2$	$Lx- = Lx+ = L/4$ $Ly- = Ly+ = L/2$ $Lz- = Lz+ = L/4$
T_{max} (°C)	86.79	86.80	86.82	86.84	86.88

temperature in PCB. Figure 2 schematically shows the computational domain, and Table 2 shows the numerical results.

T_{max} in Table 2 is the maximum temperature of the PCB. As shown in Table 2, when the computational domain is larger than the case of $Lx = Lz = L$ and $Ly = 2L$, the maximum temperature in PCB does not change significantly. Thus, in our simulation $Ly = 2L$ is specified to account for the main recirculation flow caused by the buoyancy force, and $Lx = Lz = L$ are adopted in the other two coordinates.

4.2. Grid Independence Verification

For this RBS studied, several grid systems have been tested in 0.45, 0.59, and 0.81 million cells and corresponding differences were within 1%, which indicates that the predicted results were independent of a further increase in grid density. Having established the grid independency test, further simulations were carried out on a mesh with approximately 0.59 million cells.

4.3. Computational Results Validation

Numerical simulation was conducted for the original RBS and the results agree with available test data from the manufacturer quite well. The maximum PCB temperature occurred around the 20 W A-type chip, and the deviation between the test data of T_{max} and the predicted value is about 3%. This deviation can be regarded as acceptable, which verifies the feasibility and reliability of the proposed models and the adopted numerical techniques.

5. COOLING SYSTEM IMPROVEMENTS BY NUMERICAL DESIGN

5.1. Fin Number Improvement

A plate fin heat sink is adopted for cooling the RBS, and the material of the heat sink is Al-extruded ($\lambda = 205\,\mathrm{W/(m \cdot K)}$). For the increasing heat dissipation area, fins are also installed on the EMC side, called an EMC heat sink, which is shown in Figure 3*a*. For the size of the heat sink required, the effect of fin number of aluminum heat sink with fin thickness of 1 mm is investigated and the numerical results are shown in Figure 3*b*. From the figure, it can be obviously seen that the profile of the two curves has a crucible-shape. Such variation trend of T_{max} with fin number can be interpreted as follows. The increase in fin number can expand the heat dissipation area, while the reduction of the space between two adjacent fins may deteriorate the natural convection. Thus, there exists an optimum fin number

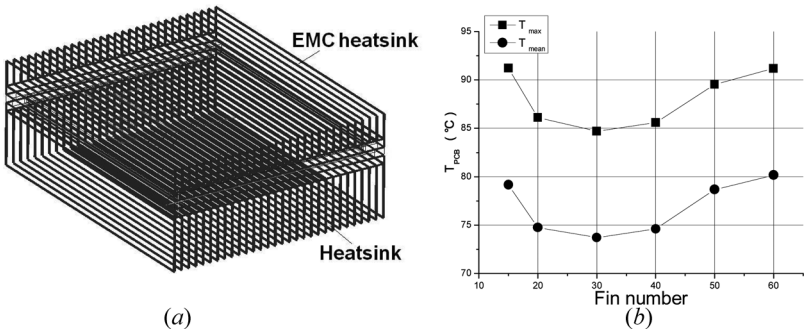


Figure 3. Heat sink improvement. (*a*) Sketch map of heat sink and EMC heat sink; and (*b*) fin number improvement.

at which the total heat transfer rate is the maximum, which leads to the minimum value of T_{max} or T_{mean}. From this investigation, 30 is adopted as the optimized fin number of the heat sink. Configuration parameters of the two heat sinks are listed in Table 3.

5.2. Heat Sink Conduction Rod

Even though an EMC heat sink is applied for increasing the area of heat dissipation, it is still found that the temperature difference between the two heat sinks is relatively large by our preliminary simulation. For reducing the temperature difference between two heat sinks, they are connected by four copper rods in between to achieve a better thermal contact between the two heat sinks, as shown in Figure 4*a*. The numerical results with and without heat sink conduction rods are pictured in Figure 4*b*, where the thermal conductivity of the copper rod is taken as $387.6\,\mathrm{W/m \cdot K}$. It can be seen that the heat sink conduction rod can reduce temperature difference between the two heat sinks; especially, the mean temperature and the T_{max} of the PCB are decreased appreciably. In the simulation, the contact between the copper rod and the heat sink is assumed perfect.

Multiple heat sinks become more familiar for high power and performance of RBS. From the above example, it may be concluded that thermal balance of heat sinks, or rather reduction of the temperature difference among heat sinks, is a useful technique to enhance heat dissipation efficiency.

Table 3. Configuration parameter of heat sink

Item	Heat sink	EMC heat sink
Base board size (mm^3)	$340 \times 275 \times 10$	$340 \times 275 \times 8$
Fin height (mm)	65	40
Fin number	30	30
Fin thickness (mm)	1.0	1.0
Fin spacing (mm)	8.45	8.45

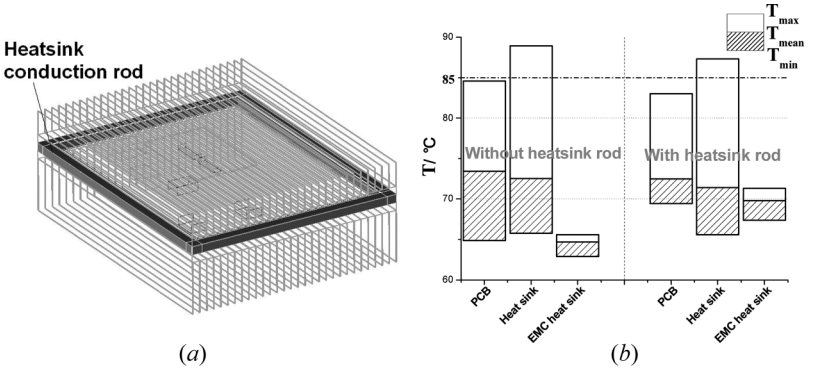


Figure 4. Heat sink conduction rod. (*a*) Diagrammatic sketch of heat sink conduction rod; and (*b*) effect of heat sink conduction rod.

5.3. Chip Conduction Rod

The top of the chips enclosed in the EMC are originally separated from the cover inner surface; hence, thermal resistance exists between the chip top surface and the inner surface of the EMC. For enhancing heat dissipaton of the chips, copper chip conduction rods are also used to build a bridge between the chip top and the EMC inner surface, as shown in Figure 5*a*. The 60 W chip and 3.6 W chip cannot be connected with a conduction rod because these two chips cannot be pressed. The cross-section sizes of the conduction rod are the same as the size of the chips. Numerical results of PCB temperature with or without the chip conduction rod are shown in Figure 5*b*. It can be seen that the maximum temperatures of both the PCB and 20 W chip decrease around 1.3°C–1.5°C.

A one-dimensional thermal resistance estimation may be helpful to understand the above results. From the geometry parameters and thermal conductivities (chip packaging material $-0.2\,\mathrm{W/(K\cdot m)}$, air gap $-0.026\,\mathrm{W/(K\cdot m)}$, and copper conduction rod $-387.6\,\mathrm{W/(K\cdot m)}$) the following three estimated thermal resistances can be obtained: chip packaging material −83°C/W; air gap −1490°C/W; and conduction rod −0.10°C/W. The thermal resistances of chip material and the air gap/conduc-

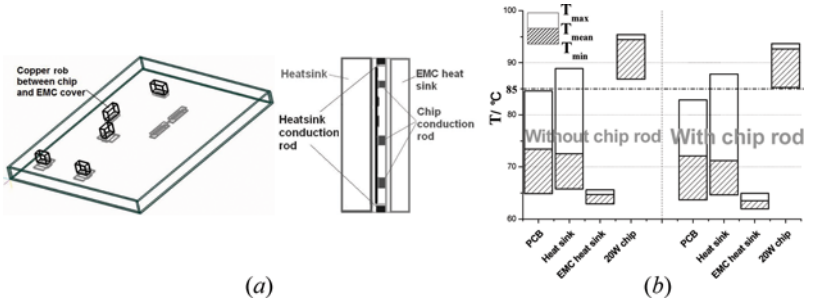


Figure 5. Chip conduction rod. (*a*) Schematic of chip conduction rod; and (*b*) effect of chip conduction rod (color figure available online).

conduction rod are in serial. Hence, the replacement of the air gap by the conduction rod significantly reduces the total thermal resistance, leading to an about 1.5°C temperature decrease in both PCB and chip; on the other hand, the relative high thermal resistance of the chip packaging material compared with that of the conduction rod restricts the function of the conduction rod.

In reference [3], it was reported that when the air gap between a high power component and system enclosure in a typical mobile phone was filled by high thermal conductivity ($120.0\,W/m \cdot K$) gap filler, appreciable cooling improvement was obtained. According to our practice, this was not only because the high thermal conductivity of the gap filler, but also the chip packaging thermal resistance itself might be comparable with the thermal resistance of the conduction rod. The above discussion implies that the chip cooling condition can be appreciably improved by using the conduction rod only when the thermal resistance of the chip packaging material is comparable to that of the conduction rod; if not, the function of the conduction rod will be restricted, and hence, not very significant. Of course the above discussion is based on the assumption that the surface contact is perfect.

5.4. Improvement of Sun Shield

For an RBS working outside, solar radiation may sometimes be strong enough to severely deteriorate its thermal condition or even to damage it. Figure 6 shows hourly incident solar radiation on surfaces at different orientations during a summer day at mid-latitudes [17]. A rough estimation can be conducted as follows. For example, assuming the exposed surface area of radio station insulation is $0.2\,m^2$, the solar irradiation intensity is $1000\,W/m^2$ and the surface emissivity of RBS is 0.7. Then, the heat absorbed by the RBS would reach 140 W, a quantity almost equal or even bigger than, its total thermal load. Thus, the sun shield has to be considered to shield the sun radiation.

However, the design of the sun radiation shield has to be taken carefully. This is because the shield may shelter from the self-radiation of the RBS to the environment while it shields the irradiation from the environment. The structure of the original sun shield is shown in Figure 7*a*, which is referred to as the plate sun shield hereafter.

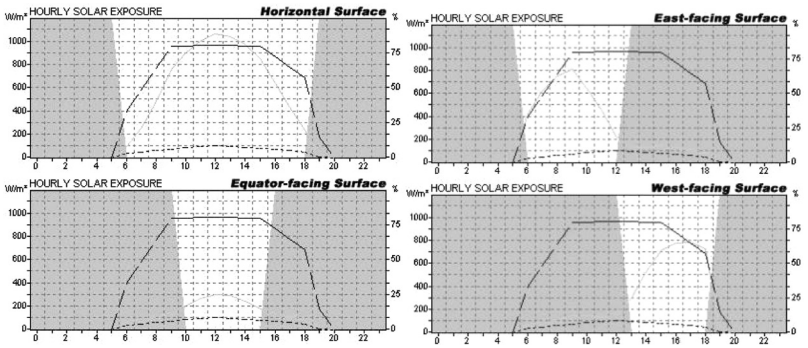


Figure 6. Graphs of solar radiation on surfaces at different orientations on a summer day at mid-latitudes [17].

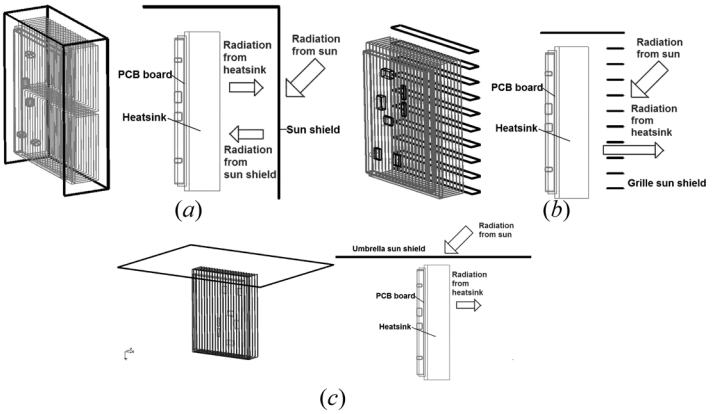


Figure 7. Schematic diagram of three types of sun shield. (*a*) Original sun shield, (*b*) grille sun shield, and (*c*) umbrella sun shield.

Furthermore, the plate sun shield blocks outside air going inside it and obstructs inside air exchanging with ambient, thus influencing the cooling effect of the heat sink.

From the above discussion it is quite clear that the plate sun shield, such as the one shown in Figure 7*a*, has two drawbacks. First, while it shields the sun irradiation it also block off its self radiation. In cases without the shields, the net radiation heat transfer of the RBS to ambient is estimated at about 42 W; and the irradiation of solar on the RBS is about 35 W. Second, the plate shield also deteriorates the air flow, which cools the RBS by natural convection.

For overcoming the disadvantages of the plate sun shield, two new types of sun shield, the grille and umbrella sun shields, respectively, are designed (see Figure 7*b* and 7*c*). These two types of shield have the following features in common. First, while they can effectively shield the sun irradiation (from top to down), the RBS self-radiation is hardly obstructed. Second, air can flow though the slot of the grille

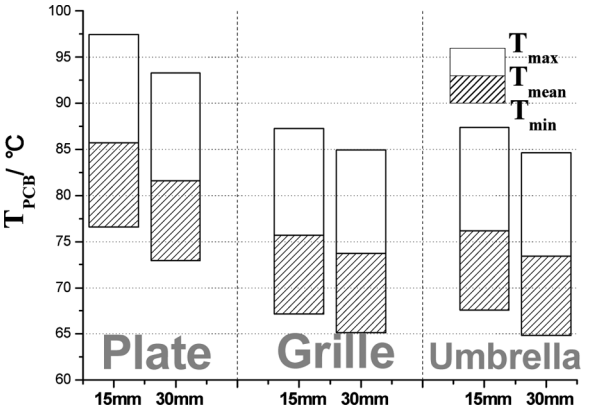


Figure 8. Sun shield performance comparison.

sun shield and mix with ambient; and in the case of the umbrella sun shield, the heat sink can also dissipate heat to ambient by natural convection.

The comparison of numerically predicted heat dissipation of the three types of sun shield are described in Figure 8, where 15 mm and 30 mm represent the distance between the sun shield to RBS. It can be seen that temperature of the PCB is appreciably lower when the grille and umbrella sun shields are used, with the umbrella sun shield being the best. For the two space distances studied, the larger space between the radio station and shield have better shield effect. The above numerical results are obtained under the following conditions: solar radiation intensity was taken as $1.120\,\mathrm{kW/m^2}$, which China is from national standard of China [18].

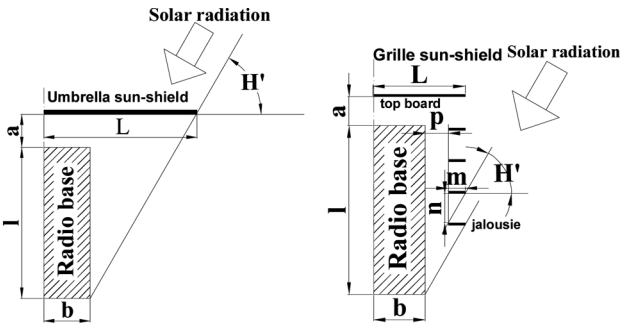
The drawbacks of the grille sun shield is the complexity of manufacturing and that of the umbrella sun shield is the larger space occupation. For the two types of new shield, apart from the space distance between the shield and RBS, some other variables should be taken into account in thermal design, and they are as follows.

The general design principle of the sun shield is to obstruct sun radiation as much as possible with an acceptable cost. Solar radiation intensity is strongly dependent on the sun elevation angle; that is, the angle between the direction of the sun and the (idealized) horizon [19]. Generally, a larger sun elevation angle will have stronger solar radiation intensity. At midday, the sun elevation angle and intensity of solar radiation are relatively high, and the design of the sun shield should take this situation into account. So the sun shield must take its effect when solar radiation is intense enough to damage RBS during 9 AM–3 PM, corresponding to a critical elevation angle H′ (see Figure 9); that is, the sun shield should block off solar radiation of the elevation angle no less than H′.

For the umbrella sun shield (see Figure 9*a*), the structure design of the umbrella sun shield should satisfy the following condition.

$$L \geq b + (1 + a)/\tan \mathrm{H}' \tag{4a}$$

For the grille sun shield (see Figure 9*b*), the length of jalousie, denoted by m, and the space between jalousies, n, have the following relationship.



(*a*) Umbrella sun shield (*b*) Grille sun shield

Figure 9. Solar radiation protection deign of sun shield. (*a*) Umbrella sun shield and (*b*) grille sun shield.

$$n = m \cdot \tan \mathrm{H}' \tag{4b}$$

The number of jalousie(s) is calculated in the following equation.

$$S = (1 + a)/(n + q)(\text{rounding}) \tag{5a}$$

The length of top board is calculated by the following.

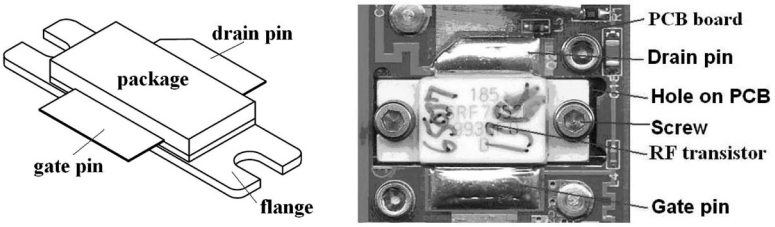
$$L \geq b + p + m \tag{5b}$$

where q is the jalousie plate thickness, and p is the distance between the radio bases and jalousie, which is usually determined by experience or operating condition.

5.5. Heat Insulation Cavity

The chip of the highest power on the PCB, i.e., the chip of 60 W, is a PF power field effect transistor amplifier and its heat flux is $3.33 \times 10^5\,\mathrm{W/m^2}$, which is the biggest challenge of heat dissipation of the radio base station. Structure and installation method of the transistor can be seen in Figure 10. The transistor is connected with the PCB by drain and gate pins, and the flange of the transistor is attached to the heat sink by two screws through a hole of the PCB. Power and temperature of the transistor are relatively high, so it is not in contact with the PCB directly except for the two pins. The thickness of the gate and drain pins is approximately 0.1 mm, which is small enough to be neglected where heat conduction is concerned. The total heat of the transistor can be considered as conduct to the heat sink only through the flange. Numerically predicted temperature distribution around the transistor is presented in Figure 11. The four blanks in Figure 11 are holes on the PCB to install transistors. From the figure, it can be seen that the temperature around the transistor on the back side of the PCB is higher than that of the chip side, and a high temperature region in the PCB appears hithermost the transistor. This is caused by the fact that the transistor does not contact the PCB directly; hence, the heat dissipated is first conducted to the heat sink, then from the heat sink to the PCB. This conduction process is schematically presented in Figure 12*a*. As the results show the local region around the transistor on the PCB is the hot spot.

As analyzed above, the high temperature region in the PCB around the transistor does not result from the transistor directly, but from the hot part of the heat



(*a*) (*b*)

Figure 10. Structure diagram of a PF power field effect transistor. (*a*) Transistor and (*b*) board with a transistor.

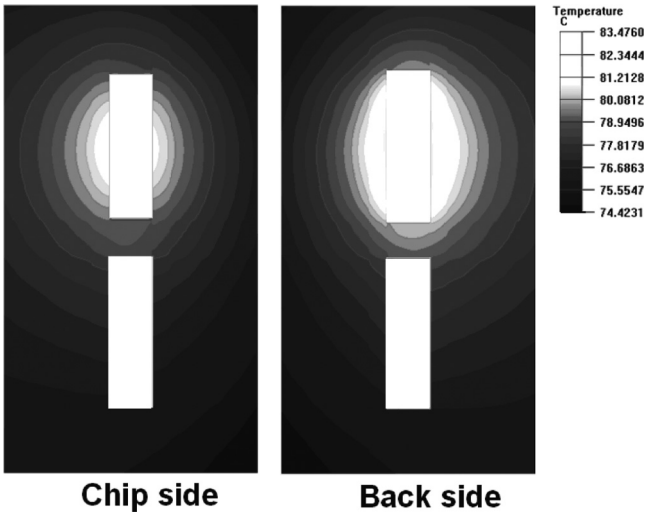


Figure 11. Temperature distribution near the 60 W chip of the original design.

sink heated by the transistor and attached by the PCB. Therefore, if the high temperature area of the heat sink is insulated from the PCB, the temperature of the hot spot in the PCB might be reduced. Based on this consideration, we proposed to excavate a cavity around the 60 W chip in the base plate of the heat sink (see

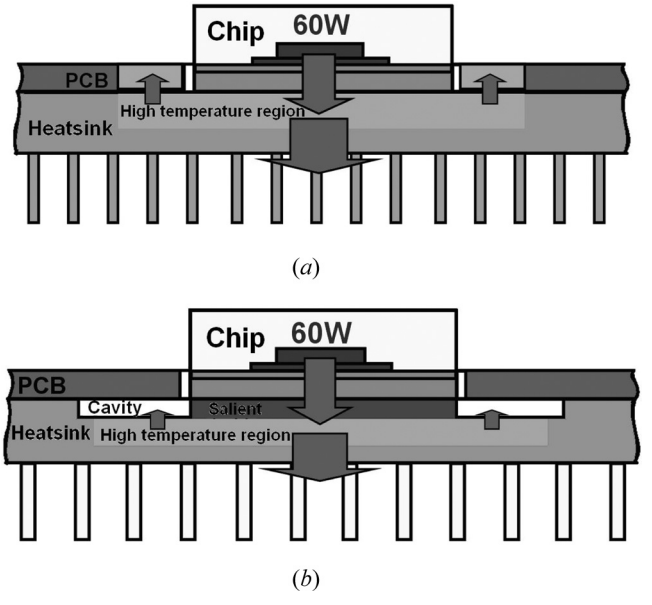


Figure 12. Schematic heat conduction route. (*a*) Schematic heat conduction route of the 60 W chip in the original design; (*b*) schematic heat conduction route of the 60 W chip with heat insulation cavity.

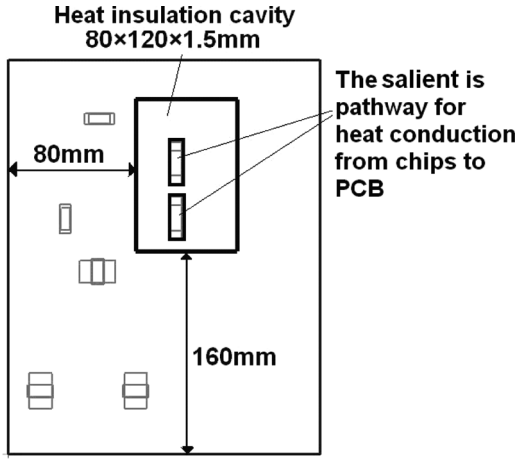


Figure 13. Position and dimension of the insulation cavity.

Figure 12*b*). Via some preliminary simulation, the final position and dimension of the excavated insulation cavity near the transistor are shown in Figure 13. The simulation results of the insulation cavity effect on the PCB temperature distribution are provided in Figure 14. It can be seen from the two figures that the insulation cavity can decrease local temperature around the transistor. Temperature distributions of the two sides of the PCB are almost identical. In Figure 14*a* we can also find that the temperature of the 60 W transistor is increased when cavity is applied because the existence of the cavity prevents the heat dissipaton of the transistors to some extent. As indicated above, an effective reduction of PCB temperature, or solder joint temperature, is the key of the thermal management for the problem studied and the chip can bear relatively higher temperature; maximum operating junction temperature of the RF power field effect transistor is allowed as high as +200°C. So, the scheme of insulation cavity in the board is effective and acceptable.

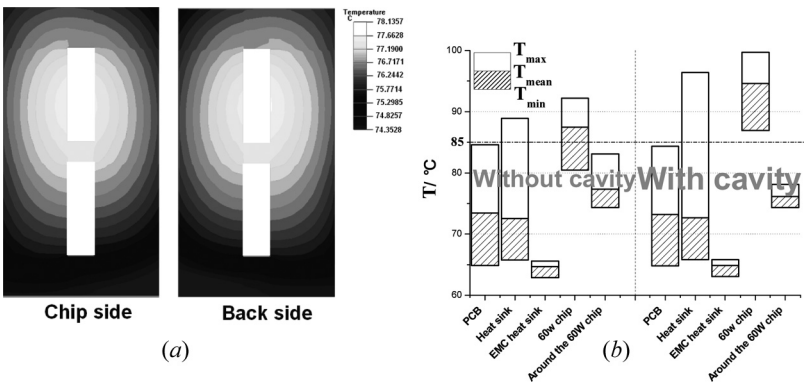


Figure 14. Effect of the heat insulation cavity.

Table 4. Simulation results of the PCB temperature of the improved and original designs

Item	T min (°C)	T max (°C)	T mean (°C)
Improved design	69.29	83.11	72.32
Original production	70.20	86.81	74.93

5.6. Integration of the Improvements and the Corresponding Numerical Results

The integrated improved thermal design of the RBS is as follows. A thirty fins heat sink is attached to the back of the PCB and the EMC heat sink is applied at the chip side; the two aluminum heat sinks are connected by a copper conduction rod. The umbrella sun shield and heat insulation cavity are used. The simulation results of the integrated improved design are shown in Table 4. It can be seen that the highest temperature on the PCB is 83.11°C in the improved design, which is below the required top limit of 85°C. In Table 4, we also list simulation results of the original production, which has a 19 fins heat sink with a bigger base plate as $411 \times 344 \times 10$ mm, 42 mm fin height, 2.45 mm fin thickness, and a plate sun shield. We can see that the new design has a better cooling effect and smaller size.

6. CONCLUSION

Several improvement methods are discussed here to enhance the effect and efficiency of a passive heat dissipating scheme so that the maximum PCB temperature can be limited below a pre-specified value. Some conclusions can be drawn as follows.

1. Thermal balance of heat sinks or reduction of temperature difference among heat sinks is useful to enhance heat dissipation efficiency.
2. The sun shield should be designed in accordance with the critical sun elevation angle to block solar radiation at the most severe condition.
3. When a high power element does not directly contact the PCB and is cooled by a heat sink attached to it, part of the heat power is transported to the PCB via conduction from the heat sink. The PCB temperature around the element may be quite high. In order to reduce the temperature in this local region, some insulation cavity in the PCB around the element may be adopted with a punishment of some increase in the chip element temperature.
4. When a chip is enclosed with an encapsulation with empty space between the top surface of the chip and the inner surface of the encapsulation, a conduction rod between the two surfaces may be appreciably helpful to improve the chip cooling, provided that the thermal resistances of both the conduction rod and the chip packaging material are comparable.

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